EXHIBIT 6

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC.,	)	
Plaintiff/Counterclaim Defendant,	)	
v.	)	Civil Action No. 04-875-GMS
	)	**CONFIDENTIAL INFORMATION PURSUANT TO PROTECTIVE ORDER**
LUCENT TECHNOLOGIES INC.,	)	
Defendant/Counterclaim Plaintiff.	)	

LUCENT TECHNOLOGIES INC.'S OBJECTIONS AND FOURTH SUPPLEMENTAL RESPONSE TO TELCORDIA TECHNOLOGIES, INC.'S INTERROGATORY NO. 6

Pursuant to FEDERAL RULES OF CIVIL PROCEDURE 26(d) and 33, Defendant/Counterclaim Plaintiff Lucent Technologies Inc. ("Lucent") by its attorneys, hereby objects and responds to Interrogatory No. 6 of Plaintiff/Counterclaim Defendant Telcordia Technologies, Inc.'s ("Telcordia") First Set of Interrogatories (the "Interrogatories") as follows:

GENERAL OBJECTIONS

Lucent incorporates by reference its General Objections in Lucent's Objections and Supplemental Responses to Telcordia Technologies, Inc.'s First Set of Interrogatories.

INTERROGATORIES

INTERROGATORY NO. 6

For each prior art reference that Lucent contends, whether taken separately or in combination, invalidates any claim of the Patent-In-Suit under 35 U.S.C. §§ 102 or 103, identify: (a) each claim in the Patent-In-Suit that Lucent contends is invalidated by the reference(s); (b) each fact known by Lucent that supports or refutes its contentions that each and every claim element or limitation is disclosed or suggested by specific teachings in the prior art reference; (c) all current or former officers, employees, agents, and consultants retained by or for Lucent who are most knowledgeable about each identified item of prior art and its relationship to the Patent-In-Suit; and (d) all documents relating to such prior art or Lucent's contentions.

THIRD SUPPLEMENTAL RESPONSE

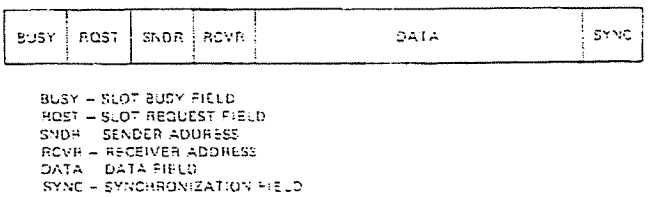
Lucent repeats and realleges all previous General Objections to Telcordia's Interrogatories and the Specific Objections to Interrogatory No. 6, and Lucent incorporates by reference its previous responses to Interrogatory No. 6.

Lucent also incorporates by reference Cisco's responses to Telcordia's Interrogatory No. 5 in *Telcordia Technologies, Inc. v. Cisco Systems, Inc.*, Civil Action No. 04-876 (GMS) (D. Del.).

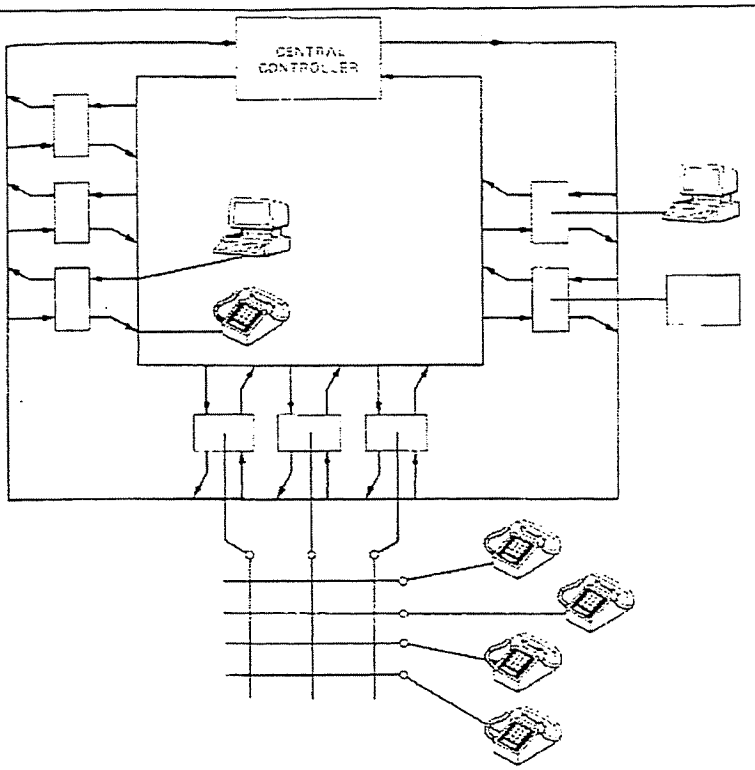
Subject to and without waiving the foregoing objections, Lucent states that at least the following additional prior art references each anticipate the asserted claims of the '306 patent and render them invalid under 35 U.S.C. § 102. In the following claim charts, Lucent uses the same application of the claims to the prior art references as Telcordia uses in its analysis of the allegedly infringing products, *see Telcordia Supplemental Responses to Lucent Interrogatory No. 1*:

Claim of U.S. Patent No. 4,893,306	**Disclosure in Budrikis & Netravali, "A Packet/Circuit Switch," AT&T Bell Laboratories Technical Journal, Vol. 63, No. 8, October 1984 ("Budrikis")**

1. A method for simultaneously transmitting data from sources having different bit rates in a telecommunication network comprising the steps of:	Budrikis discloses a method for simultaneously transmitting data from sources having different bit rates in a telecommunication network. *See* p. 1499 ("We propose a switch, suitable for an integrated local communications network, that will support packet switching and packet switching, with a wide range of bit rates.") *See* p. 1500 ("We propose a switch and, more generally, a new switch architecture that support within one switching fabric both circuit- and packet-switched connections.") *See* p. 1502 ("All elements of our proposal are well established and tried. Central, or stored program, control in circuit switching is over twenty years old. The idea of switching by time slot interchanges is even older, followed shortly by its realization through read-and-writes in computer memory. Packet switching is more recent, but is also well established both in local and wide-area networks.") *See* p. 1502 ("Also, our proposal is not first in its suggestion that voice and data be integrated on a common network. But it appears to be first in suggesting a common switch for circuits and packets as the basis for that integration.") *See* p. 1500 ("The cardinal components of the switch (see Fig. 1) are a pair of Serial Memories (SMs), a Central Controller (CC), and Accessing Units (AUs).")
generating a bit stream comprising a sequence of frames,	Budrikis discloses generating a bit stream comprising a sequence of frames. *See* p. 1501 ("Communications are carried on by write-and-reads in memory/time slots of uniform length and format. Each slot consists of a data fields and several control fields. Collectively, the control fields provide synchronization, "Slot busy" indication, source and destination addressing, and slot pleading.") *See* p. 1506 ("In context of our proposal, a packet used in packet-switched communication is made up of five control fields and data, as shown in Fig. 5. The same format could be used in circuit-switched packets. But for these, at least one of the two address fields is unnecessary. Its space may either be added to the data field, or it could be used as a separate channel, a companion to the main channel.")

each of said frames including a transmission overhead field containing frame timing information and an empty payload field, and	Budrikis discloses that each of the frames includes a transmission overhead field containing frame timing information and an empty payload field. *See* p. 1506 ("The six fields marked in Fig. 5 are: 1. BUSY – a single bit to indicate slot occupancy 2. RQST – a single bit, common channel used for slot pleading 3. SNDR – address or password of AU sending packet 4. RCVR – address or password of AU intended to receive packet 5. DATA – data field 6. SYNC – synchronization field. The roles of all the fields, except RQST and SYNC, are self-evident. RQST is used by packet-switching AUs and we will see its function presently when we discuss data communications. The SYNC field is written by the central controller to ensure slot and frame synchronization. Although both synchronizations could be achieved with just one bit per slot, a field of two bits will make them more secure. Altogether, the following numbers would be of the right order: BUSY and RQST one bit each, SYNC two bits, the addresses 14 bits each, and DATA 192 bits, for a total packet of 224 bits, or 28 bytes.") *See* Fig. 5:  Fig. 5—Slot format. Typically, BUSY, RQST and SYNC would be one-bit fields, the address fields could be two bytes each and the data field 24 bytes. *See* p. 1513 ("Assuming a telephone voice signal sampled at 8 kHz, represented by 8 bits per sample and an allowed delay due to packetization of 3 ms, a packet may contain 24 samples or 192 bits of data. The overheads are mainly in the address: Assuming a 10,000-voice-line switch and a total number of AUs not exceeding 16K, the SNDR and RCVR fields could be 14 bits each. As we already noted, BUSY and RQST need be only 1 bit each, and SYNC 2 bits. The total overhead will then be 32 bits and the packet length will be 224 bits.") *See* p. 1519 ("The possibility for the two modes is brought about

	by having enlarged time slots that can include addressing information, and then by making these of fixed length so that they can be made available regularly.") *See* p. 1519 ("We have proposed that data packets be fixed at 192 bits, or 24 samples of pulse-code-modulated voice. This limits the delay due to packetization to 3 ms. The total delay, which includes propagation along the memories, will then be less than 4 ms, even in a very large switch.")
filling the empty payload fields in said frames with data in packetized format from a plurality of sources which have access to the bit stream including circuit or packet sources,	Budrikis discloses filling the empty payload fields with data in packetized format from a plurality of sources which have access to the bit stream, including circuit or packet sources. *See* p. 1501 ("An AU acts as an agent of a client station (St) (e.g., telephone, facsimile terminal, computer) mediates communications between it and other stations by way of corresponding AUs.") *See* p. 1502 ("In essence, our scheme is an adaptation of seemingly diverse procedures, so that they may coexist. Time division slots are enlarged from what is usual in circuit switching, so that they can carry the control information essential to packet switching. Unlike normal packet-switched schemes, packets are of a single fixed length so that they can also be circuit-switched. Instead of separate time and space division stages, common in current telephone switches, we have a combined space/time fabric, abstracted from ring and bus networks, with a particular debt to Fasnet. This makes packet switching possible without controller intervention. Finally, the controller maintains circuit connections by repetitive slot allocations, which is only marginally different from what takes place in a time division stage of a standard switch.") *See* p. 1514 ("Another criterion by which the overall size of a packet can be decided is efficiency. Since the allowable delay for voice is binding, the best size indicated for maximum efficiency will be of interest only if it is smaller than that already decided.") *See* Fig. 2:

	 Fig. 2—Different options in AU tasking. All AUs could be of one type, each serving a single station (right); AUs could be shared by a larger group of stations requiring selector switching outside the main switch (center); or an AU could be multitasked, serving more than one type of station (left).
such that data in packetized format from any of said sources is written into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously via said bit stream.	Budrikis discloses that data in packetized format from any of the sources is written into any available empty payload field of the frames for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from said plurality of sources simultaneously via the bit stream. *See* p. 1518 ("We have proposed a switch architecture that supports circuit- and packet-switch communications. Both communications can proceed at widely varying rates: Circuits can be set up with different capacities, selectable as a binary fraction or multiple of a basic capacity, while packet-switched communications share in the pool of the total switch capacity that is not in use at any given time. Thus, the proposed switch could cater efficiently in mediating real-time signals and data. Specifically, it could be a PBX that, apart from voice, could provide other circuit- and packet-switched services.") *See* p. 1508 ("When idle, the dispatcher is normally in the "Go" state and monitors the sending buffer (for the forward channel), checking whether it contains a packet for transmission. If it does, it reads the BUSY field of the next block on the forward channel

and at the same time write a "ONE" in that field so as to sized the slot, should it be available. If it is not, i.e., BUSY was already "ONE." then it will write "ONE" in the next RQST field on the reverse channel and wait for the next BUSY field on the forward channel. It will repeat reading and writing of BUSY on the forward channel and sending RQSTs on the reverse channel until a "ZERO" BUSY occurs. It will then write in the related SNDR, RCVR, and DATA fields, so dispatching a packet."

See Fig. 7:

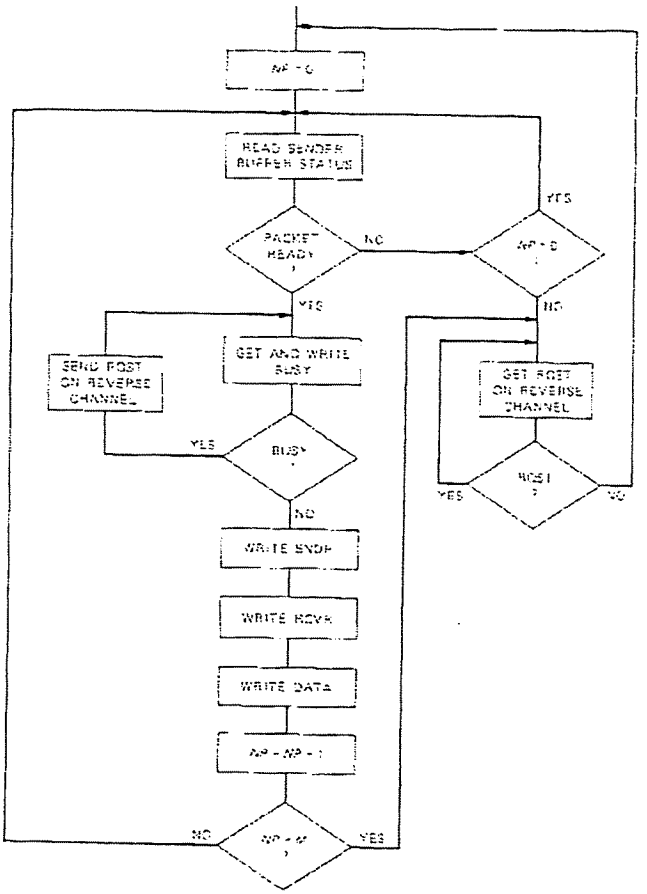
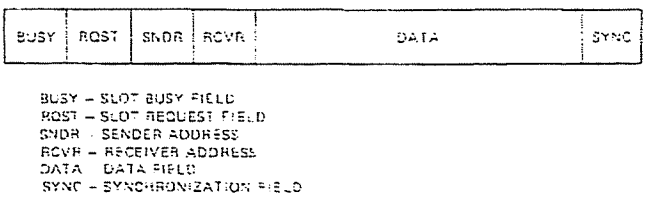


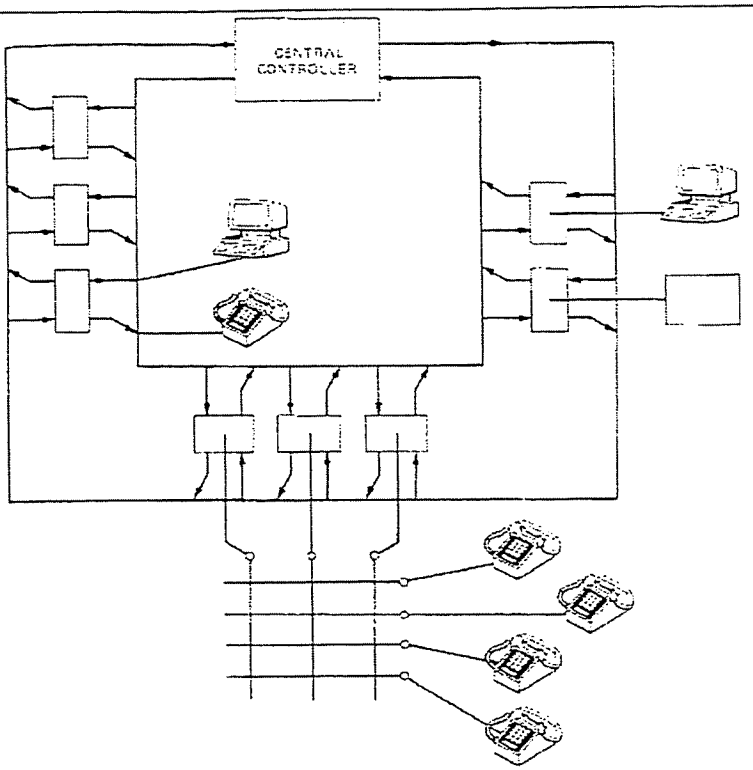
Fig. 6—Flowchart of forward channel data dispatch routine

See p. 1510 ("*M* is a parameter that may vary with AU. It represents priority standing: The larger its value, the less sensitive the AU is to pleadings for slots by other AUs that are down stream from it. It is normally set in relation to the rate of the station that the AU serves.")

3. A method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources comprising	Budrikis discloses a method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources. *See* p. 1499 ("We propose a switch, suitable for an integrated local communications network, that will support packet switching and packet switching, with a wide range of bit rates.") *See* p. 1500 ("We propose a switch and, more generally, a new switch architecture that support within one switching fabric both circuit- and packet-switched connections.") *See* p. 1502 ("All elements of our proposal are well established and tried. Central, or stored program, control in circuit switching is over twenty years old. The idea of switching by time slot interchanges is even older, followed shortly by its realization through read-and-writes in computer memory. Packet switching is more recent, but is also well established both in local and wide-area networks.") *See* p. 1502 ("Also, our proposal is not first in its suggestion that voice and data be integrated on a common network. But it appears to be first in suggesting a common switch for circuits and packets as the basis for that integration.") *See* p. 1500 ("The cardinal components of the switch (see Fig. 1) are a pair of Serial Memories (SMs), a Central Controller (CC), and Accessing Units (AUs).")
generating a bit stream comprising a sequence of frames,	Budrikis discloses generating a bit stream comprising a sequence of frames. *See* p. 1501 ("Communications are carried on by write-and-reads in memory/time slots of uniform length and format. Each slot consists of a data fields and several control fields. Collectively, the control fields provide synchronization, "Slot busy" indication, source and destination addressing, and slot pleading.") *See* p. 1506 ("In context of our proposal, a packet used in packet-switched communication is made up of five control fields and data, as shown in Fig. 5. The same format could be used in circuit-switched packets. But for these, at least one of the two address fields is unnecessary. Its space may either be added to the data field, or it could be used as a separate channel, a companion to the main channel.")

each of said frames including a transmission overhead field containing frame timing information and an empty payload field,	Budrikis discloses that each of the frames includes a transmission overhead field containing frame timing information and an empty payload field. *See* p. 1506 ("The six fields marked in Fig. 5 are: 1. BUSY – a single bit to indicate slot occupancy 2. RQST – a single bit, common channel used for slot pleading 3. SNDR – address or password of AU sending packet 4. RCVR – address or password of AU intended to receive packet 5. DATA – data field 6. SYNC – synchronization field. The roles of all the fields, except RQST and SYNC, are self-evident. RQST is used by packet-switching AUs and we will see its function presently when we discuss data communications. The SYNC field is written by the central controller to ensure slot and frame synchronization. Although both synchronizations could be achieved with just one bit per slot, a field of two bits will make them more secure. Altogether, the following numbers would be of the right order: BUSY and RQST one bit each, SYNC two bits, the addresses 14 bits each, and DATA 192 bits, for a total packet of 224 bits, or 28 bytes.") *See* Fig. 5:  Fig. 5—Slot format. Typically, BUSY, RQST and SYNC would be one-bit fields, the address fields could be two bytes each and the data field 24 bytes. *See* p. 1513 ("Assuming a telephone voice signal sampled at 8 kHz, represented by 8 bits per sample and an allowed delay due to packetization of 3 ms, a packet may contain 24 samples or 192 bits of data. The overheads are mainly in the address: Assuming a 10,000-voice-line switch and a total number of AUs not exceeding 16K, the SNDR and RCVR fields could be 14 bits each. As we already noted, BUSY and RQST need be only 1 bit each, and SYNC 2 bits. The total overhead will then be 32 bits and the packet length will be 224 bits.") *See* p. 1519 ("The possibility for the two modes is brought about

	by having enlarged time slots that can include addressing information, and then by making these of fixed length so that they can be made available regularly.") *See* p. 1519 ("We have proposed that data packets be fixed at 192 bits, or 24 samples of pulse-code-modulated voice. This limits the delay due to packetization to 3 ms. The total delay, which includes propagation along the memories, will then be less than 4 ms, even in a very large switch.")
packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets, and	Budrikis discloses packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets. *See* p. 1501 ("An AU acts as an agent of a client station (St) (e.g., telephone, facsimile terminal, computer) mediates communications between it and other stations by way of corresponding AUs.") *See* p. 1502 ("In essence, our scheme is an adaptation of seemingly diverse procedures, so that they may coexist. Time division slots are enlarged from what is usual in circuit switching, so that they can carry the control information essential to packet switching. Unlike normal packet-switched schemes, packets are of a single fixed length so that they can also be circuit-switched. Instead of separate time and space division stages, common in current telephone switches, we have a combined space/time fabric, abstracted from ring and bus networks, with a particular debt to Fasnet. This makes packet switching possible without controller intervention. Finally, the controller maintains circuit connections by repetitive slot allocations, which is only marginally different from what takes place in a time division stage of a standard switch.") *See* p. 1514 ("Another criterion by which the overall size of a packet can be decided is efficiency. Since the allowable delay for voice is binding, the best size indicated for maximum efficiency will be of interest only if it is smaller than that already decided.") *See* Fig. 2:

	 Fig. 2—Different options in AU tasking. All AUs could be of one type, each serving a single station (right); AUs could be shared by a larger group of stations requiring selector switching outside the main switch (center); or an AU could be multitasked, serving more than one type of station (left).
inserting said packets from said sources into the empty payload fields of said frames such that a packet from any of said sources is inserted into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously using said bit stream.	Budrikis discloses that data in packetized format from any of the sources is inserted into any available empty payload field of the frames for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from the plurality of sources simultaneously via the bit stream. *See* p. 1518 ("We have proposed a switch architecture that supports circuit- and packet-switch communications. Both communications can proceed at widely varying rates: Circuits can be set up with different capacities, selectable as a binary fraction or multiple of a basic capacity, while packet-switched communications share in the pool of the total switch capacity that is not in use at any given time. Thus, the proposed switch could cater efficiently in mediating real-time signals and data. Specifically, it could be a PBX that, apart from voice, could provide other circuit- and packet-switched services.") *See* p. 1508 ("When idle, the dispatcher is normally in the "Go" state and monitors the sending buffer (for the forward channel), checking whether it contains a packet for transmission. If it does, it reads the BUSY field of the next block on the forward channel

and at the same time write a "ONE" in that field so as to sized the slot, should it be available. If it is not, i.e., BUSY was already "ONE." then it will write "ONE" in the next RQST field on the reverse channel and wait for the next BUSY field on the forward channel. It will repeat reading and writing of BUSY on the forward channel and sending RQSTs on the reverse channel until a "ZERO" BUSY occurs. It will then write in the related SNDR, RCVR, and DATA fields, so dispatching a packet."

See Fig. 7:

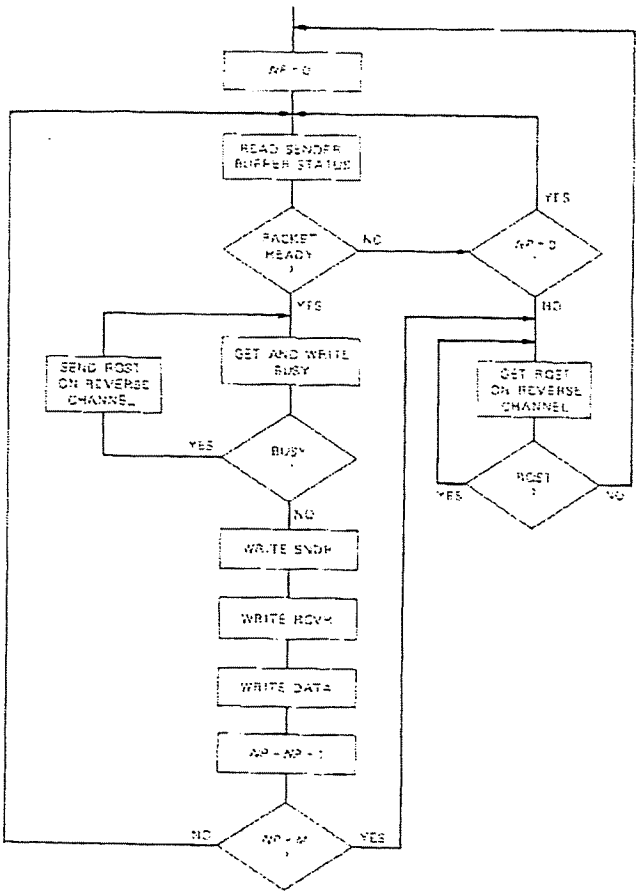


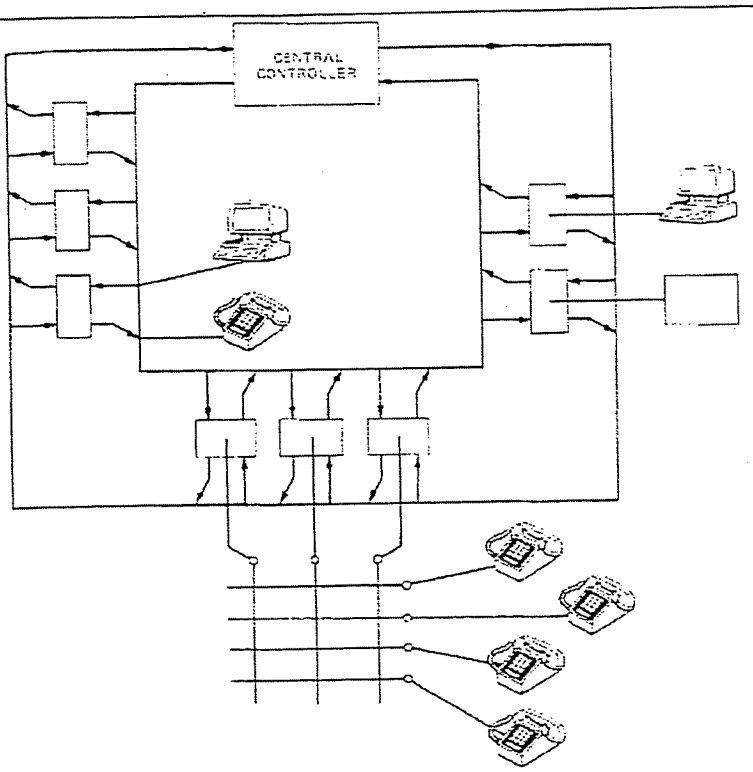
Fig. 6—Flowchart of forward channel data dispatch routine

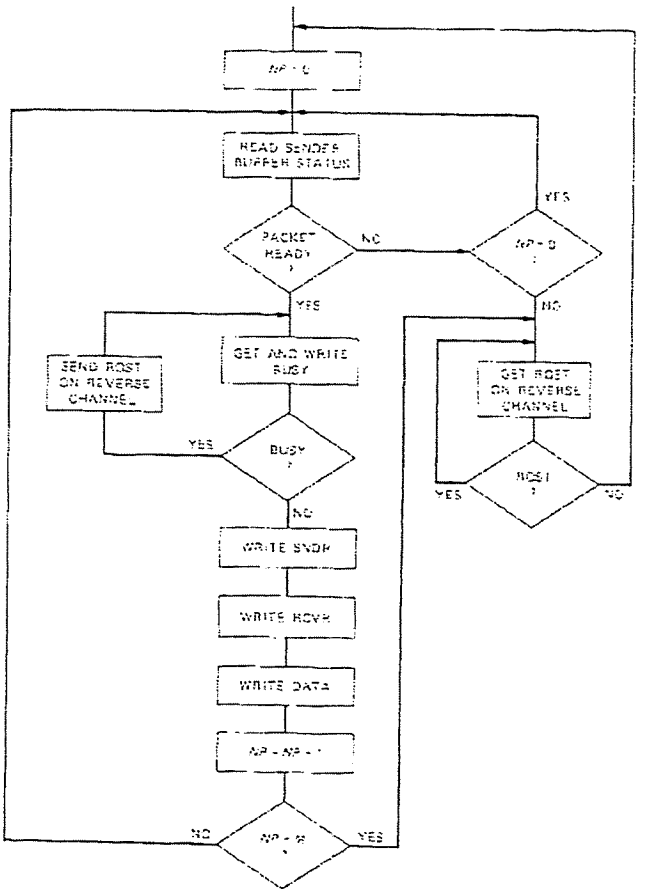
See p. 1510 ("*M* is a parameter that may vary with AU. It represents priority standing: The larger its value, the less sensitive the AU is to pleadings for slots by other AUs that are down stream from it. It is normally set in relation to the rate of the station that the AU serves.")

4. An apparatus for assembling a dynamic time division multiplexing bit stream comprising,	Budrikis discloses an apparatus for assembling a dynamic time division multiplexing bit stream. *See* p. 1499 ("We propose a switch, suitable for an integrated local communications network, that will support packet switching and packet switching, with a wide range of bit rates.") *See* p. 1500 ("We propose a switch and, more generally, a new switch architecture that support within one switching fabric both circuit- and packet-switched connections.") *See* p. 1502 ("All elements of our proposal are well established and tried. Central, or stored program, control in circuit switching is over twenty years old. The idea of switching by time slot interchanges is even older, followed shortly by its realization through read-and-writes in computer memory. Packet switching is more recent, but is also well established both in local and wide-area networks.") *See* p. 1502 ("Also, our proposal is not first in its suggestion that voice and data be integrated on a common network. But it appears to be first in suggesting a common switch for circuits and packets as the basis for that integration.") *See* p. 1500 ("The cardinal components of the switch (see Fig. 1) are a pair of Serial Memories (SMs), a Central Controller (CC), and Accessing Units (AUs).")
generating means for generating a train of frames	Budrikis discloses a generating means for generating a train of frames. *See* p. 1501 ("Communications are carried on by write-and-reads in memory/time slots of uniform length and format. Each slot consists of a data fields and several control fields. Collectively, the control fields provide synchronization, "Slot busy" indication, source and destination addressing, and slot pleading.") *See* p. 1506 ("In context of our proposal, a packet used in packet-switched communication is made up of five control fields and data, as shown in Fig. 5. The same format could be used in circuit-switched packets. But for these, at least one of the two address fields is unnecessary. Its space may either be added to the data field, or it could be used as a separate channel, a companion to the main channel.")
wherein each frame	Budrikis discloses an apparatus wherein each frame includes a

includes a transmission overhead field containing timing information and an empty payload field,	transmission overhead field containing timing information and an empty payload field. *See* p. 1506 ("The six fields marked in Fig. 5 are: 1. BUSY – a single bit to indicate slot occupancy 2. RQST – a single bit, common channel used for slot pleading 3. SNDR – address or password of AU sending packet 4. RCVR – address or password of AU intended to receive packet 5. DATA – data field 6. SYNC – synchronization field. The roles of all the fields, except RQST and SYNC, are self-evident. RQST is used by packet-switching AUs and we will see its function presently when we discuss data communications. The SYNC field is written by the central controller to ensure slot and frame synchronization. Although both synchronizations could be achieved with just one bit per slot, a field of two bits will make them more secure. Altogether, the following numbers would be of the right order: BUSY and RQST one bit each, SYNC two bits, the addresses 14 bits each, and DATA 192 bits, for a total packet of 224 bits, or 28 bytes.") *See* Fig. 5:  BUSY – SLOT BUSY FIELD RQST – SLOT REQUEST FIELD SNDR – SENDER ADDRESS RCVR – RECEIVER ADDRESS DATA – DATA FIELD SYNC – SYNCHRONIZATION FIELD Fig. 5—Slot format. Typically, BUSY, RQST and SYNC would be one-bit fields, the address fields could be two bytes each and the data field 24 bytes. *See* p. 1513 ("Assuming a telephone voice signal sampled at 8 kHz, represented by 8 bits per sample and an allowed delay due to packetization of 3 ms, a packet may contain 24 samples or 192 bits of data. The overheads are mainly in the address: Assuming a 10,000-voice-line switch and a total number of AUs not exceeding 16K, the SNDR and RCVR fields could be 14 bits each. As we already noted, BUSY and RQST need be only 1 bit each, and SYNC 2 bits. The total overhead will then be 32 bits and the packet length will be 224 bits.") *See* p. 1519 ("The possibility for the two modes is brought about by having enlarged time slots that can include addressing

	information, and then by making these of fixed length so that they can be made available regularly.") *See* p. 1519 ("We have proposed that data packets be fixed at 192 bits, or 24 samples of pulse-code-modulated voice. This limits the delay due to packetization to 3 ms. The total delay, which includes propagation along the memories, will then be less than 4 ms, even in a very large switch.")
processing means for processing data from a plurality of sources into packet format, and	Budrikis discloses an apparatus for processing data from a plurality of sources into packet format. *See* p. 1501 ("An AU acts as an agent of a client station (St) (e.g., telephone, facsimile terminal, computer) mediates communications between it and other stations by way of corresponding AUs.") *See* p. 1502 ("In essence, our scheme is an adaptation of seemingly diverse procedures, so that they may coexist. Time division slots are enlarged from what is usual in circuit switching, so that they can carry the control information essential to packet switching. Unlike normal packet-switched schemes, packets are of a single fixed length so that they can also be circuit-switched. Instead of separate time and space division stages, common in current telephone switches, we have a combined space/time fabric, abstracted from ring and bus networks, with a particular debt to Fasnet. This makes packet switching possible without controller intervention. Finally, the controller maintains circuit connections by repetitive slot allocations, which is only marginally different from what takes place in a time division stage of a standard switch.") *See* p. 1514 ("Another criterion by which the overall size of a packet can be decided is efficiency. Since the allowable delay for voice is binding, the best size indicated for maximum efficiency will be of interest only if it is smaller than that already decided.") *See* Fig. 2:

	 Fig. 2—Different options in AU tasking. All AUs could be of one type, each serving a single station (right); AUs could be shared by a larger group of stations requiring selector switching outside the main switch (center); or an AU could be multitasked, serving more than one type of station (left).
inserting means for receiving said train of frames and for inserting each of said packets comprised of data from one of said plurality of sources into any empty payload field of any of said frames available to said inserting means to form said bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources	Budrikis discloses an apparatus with an inserting means for receiving a train of frames and for inserting packets comprised of data from one of a plurality of sources into any empty payload field of any of the frames available to the inserting means to form a bit stream so that data from each source can be transmitted at its own desired bit rate via the bit stream and so that data from the plurality of sources can be transmitted simultaneously via the bit stream. *See* p. 1518 ("We have proposed a switch architecture that supports circuit- and packet-switch communications. Both communications can proceed at widely varying rates: Circuits can be set up with different capacities, selectable as a binary fraction or multiple of a basic capacity, while packet-switched communications share in the pool of the total switch capacity that is not in use at any given time. Thus, the proposed switch could cater efficiently in mediating real-time signals and data. Specifically, it could be a PBX that, apart from voice, could provide other circuit- and packet-switched services.") *See* p. 1508 ("When idle, the dispatcher is normally in the "Go"

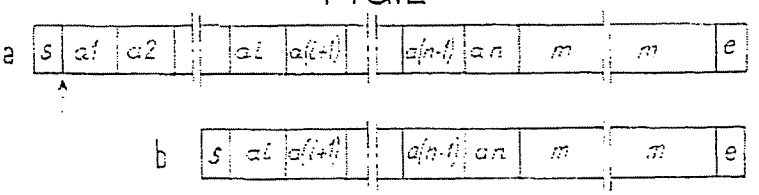
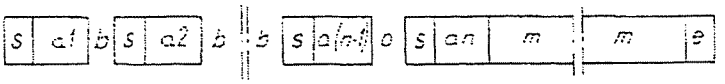
can be transmitted simultaneously via said bit stream.	state and monitors the sending buffer (for the forward channel), checking whether it contains a packet for transmission. If it does, it reads the BUSY field of the next block on the forward channel and at the same time write a "ONE" in that field so as to sized the slot, should it be available. If it is not, i.e., BUSY was already "ONE." then it will write "ONE" in the next RQST field on the reverse channel and wait for the next BUSY field on the forward channel. It will repeat reading and writing of BUSY on the forward channel and sending RQSTs on the reverse channel until a "ZERO" BUSY occurs. It will then write in the related SNDR, RCVR, and DATA fields, so dispatching a packet." *See* Fig. 7:  Fig. 6—Flowchart of forward channel data dispatch routine. *See* p. 1510 ("*M* is a parameter that may vary with AU. It represents priority standing: The larger its value, the less sensitive the AU is to pleadings for slots by other AUs that are down stream from it. It is normally set in relation to the rate of

	the station that the AU serves.")

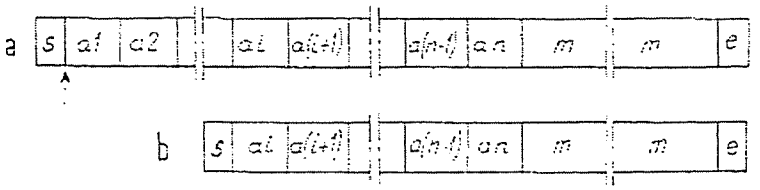
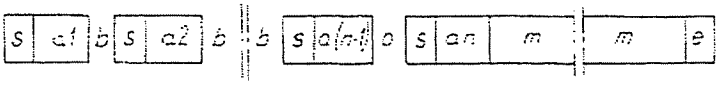
Claim of U.S. Patent No. 4,893,306	Disclosure in U.S. Patent No. 4,577,311 ("the '311 Patent")
1. A method for simultaneously transmitting data from sources having different bit rates in a telecommunication network comprising the steps of:	The '311 Patent discloses a method for simultaneously transmitting data from sources having different bit rates in a telecommunication network. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and, more particularly, a packet-switching network of the multiservice type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Consideration will first be turned toward FIG. 1 which shows a portion of a nodal telecommunication system comprising, in its complete state: a plurality of subscriber stations SS each of which includes at least one terminal whether this be a telephone, a visiophone, a data transmission terminal, etc. When a station has several terminals, these can be either all the same or mixed; concentrators CO to each of which stations SS are connected through subscriber's lines SL; local exchanges LE to each of which concentrators CO are connected by concentrator links CL where these local exchanges can, moreover, be interconnected through local links LL; transit exchanges TE to each of which local exchanges LE are connected by exchange link EL, where these transit exchanges can be interconnected through transit links TL. In case the message packetizing operation is carried out in circuits housed in the stations SS, the entire system in FIG. 1 constitutes a system in accordance with the invention. If the routing digital address insertion circuits are also contained in these stations SS,

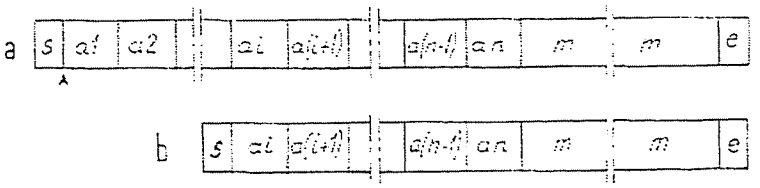
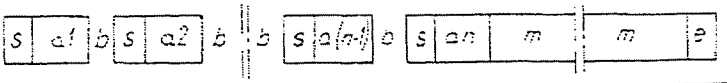
	then all the system nodes, namely concentrators CO, local exchanges LE and transit exchanges TE become switching networks in compliance with the invention and the links CL, EL and TL are input links to and output links from these switching networks. As an input link, they may have at least one channel but as an output link they must have a plurality of channels (channel group or channel bundle). However, and still within the scope of the invention, the address insertion into the addresses field can be transferred to the concentrator CO or local exchange LE level." 3:3-36.
generating a bit stream comprising a sequence of frames,	The '311 Patent discloses a method of generating a bit stream comprising a sequence of frames. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a.

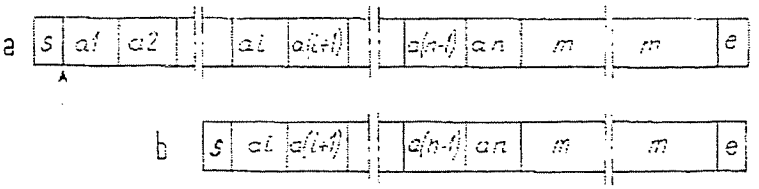
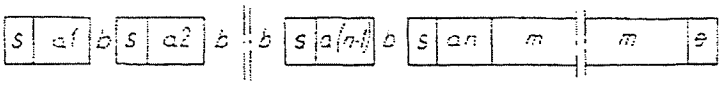
	It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit comprises means for deleting the address concerning itself in the address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its route. The address intended for a directional switching unit encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4.

	FIG.2  FIG.3 
each of said frames including a transmission overhead field containing frame timing information and an empty payload field, and	The '311 Patent discloses each of said frames including a transmission overhead field containing frame timing information and an empty payload field. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two

	versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a. It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit comprises means for deleting the address concerning itself in the address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its route. The address intended for a directional switching unit encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after

	reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
filling the empty payload fields in said frames with data in packetized format from a plurality of sources which have access to the bit stream including circuit or packet sources,	The '311 Patent discloses filling the empty payload fields in said frames with data in packetized format from a plurality of sources which have access to the bit stream including circuit or packet sources. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and, more particularly, a packet-switching network of the multiservice type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52

	"When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
such that data in packetized format from any of said sources is written into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and	The '311 Patent discloses each of said frames including a transmission overhead field containing frame timing information and an empty payload field. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to

for transmitting data from said plurality of sources simultaneously via said bit stream.	reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
3. A method for generating a bit stream capable of transporting data originating from both circuit	The '311 Patent discloses a method for generating a bit stream capable of transporting data originating from both circuit transmission and packet sources. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and,

transmission and packet sources comprising	more particularly, a packet-switching network of the multiservice type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Consideration will first be turned toward FIG. 1 which shows a portion of a nodal telecommunication system comprising, in its complete state: a plurality of subscriber stations SS each of which includes at least one terminal whether this be a telephone, a visiophone, a data transmission terminal, etc. When a station has several terminals, these can be either all the same or mixed; concentrators CO to each of which stations SS are connected through subscriber's lines SL; local exchanges LE to each of which concentrators CO are connected by concentrator links CL where these local exchanges can, moreover, be interconnected through local links LL; transit exchanges TE to each of which local exchanges LE are connected by exchange link EL, where these transit exchanges can be interconnected through transit links TL. In case the message packetizing operation is carried out in circuits housed in the stations SS, the entire system in FIG. 1 constitutes a system in accordance with the invention. If the routing digital address insertion circuits are also contained in these stations SS, then all the system nodes, namely concentrators CO, local exchanges LE and transit exchanges TE become switching networks in compliance with the invention and the links CL, EL and TL are input links to and output links from these switching networks. As an input link, they may have at least one channel but as an output link they must have a plurality of channels (channel group or channel bundle). However, and still within the scope of the invention, the address insertion into the addresses field can be transferred to the concentrator CO or local exchange LE level." 3:3-36.
generating a bit stream comprising a	The '311 Patent discloses a method of generating a bit stream comprising a sequence of frames.

sequence of frames,	"Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a. It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit comprises means for deleting the address concerning itself in the address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its

route. The address intended for a directional switching unit encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31

"When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4.

FIG.2

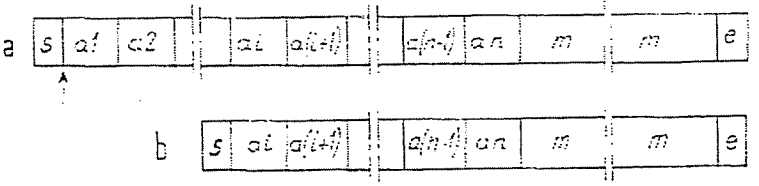
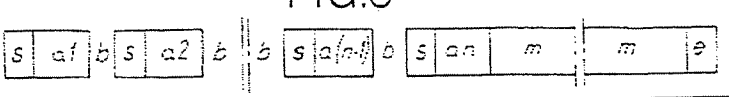
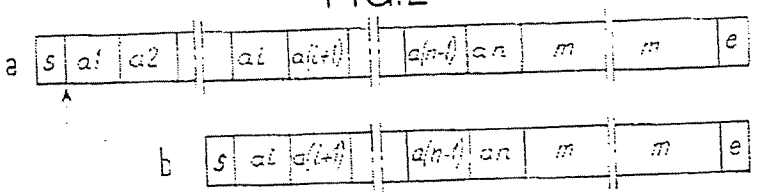
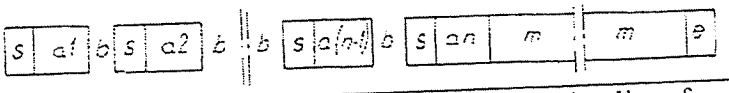


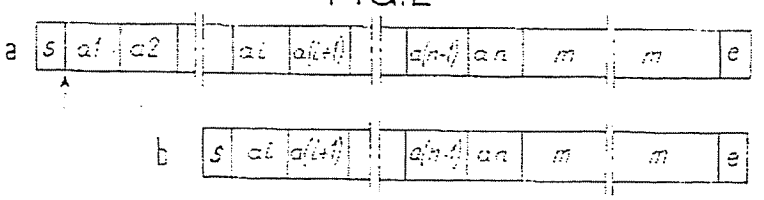
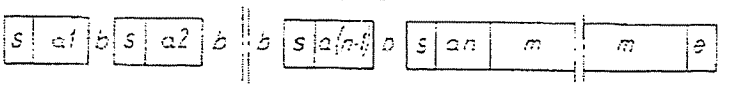
FIG.3

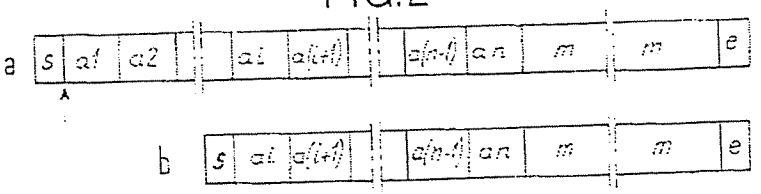
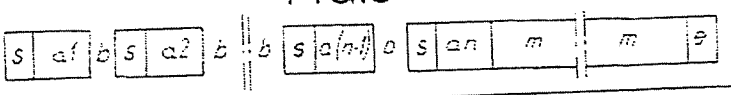


each of said frames including a transmission overhead field containing frame timing information and an empty payload field,	The '311 Patent discloses each of said frames including a transmission overhead field containing frame timing information and an empty payload field. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a. It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit

	comprises means for deleting the address concerning itself in the address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its route. The address intended for a directional switching unit encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4.

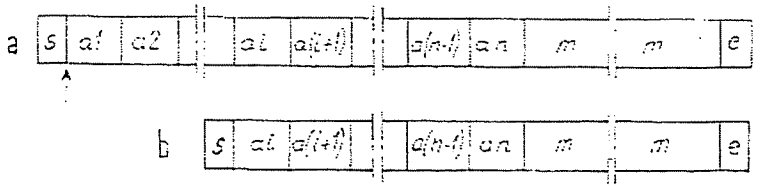
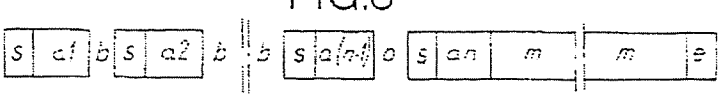
	FIG.2  FIG.3 
packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets, and	The '311 Patent discloses packetizing data from a plurality of sources having different bit rates and which have access to said bit stream including circuit transmission sources or customer premises equipment to produce data packets. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and, more particularly, a packet-switching network of the multiservice type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus

	400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
inserting said packets from said sources into the empty payload fields of said frames such that a packet from any of said sources is inserted into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and	The '311 Patent discloses inserting said packets from said sources into the empty payload fields of said frames such that a packet from any of said sources is inserted into any available empty payload field of any of said frames for transmitting data from each of said sources at its own desired bit rate via said bit stream and for transmitting data from said plurality of sources simultaneously using said bit stream. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to

for transmitting data from said plurality of sources simultaneously using said bit stream.	reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
4. An apparatus for assembling a dynamic time division multiplexing bit stream comprising,	The '311 Patent discloses an apparatus for assembling a dynamic time division multiplexing bit stream. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and, more particularly, a packet-switching network of the multiservice

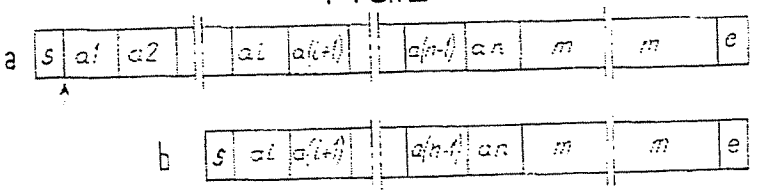
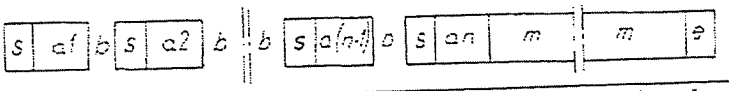
	type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Consideration will first be turned toward FIG. 1 which shows a portion of a nodal telecommunication system comprising, in its complete state: a plurality of subscriber stations SS each of which includes at least one terminal whether this be a telephone, a visiophone, a data transmission terminal, etc. When a station has several terminals, these can be either all the same or mixed; concentrators CO to each of which stations SS are connected through subscriber's lines SL; local exchanges LE to each of which concentrators CO are connected by concentrator links CL where these local exchanges can, moreover, be interconnected through local links LL; transit exchanges TE to each of which local exchanges LE are connected by exchange link EL, where these transit exchanges can be interconnected through transit links TL. In case the message packetizing operation is carried out in circuits housed in the stations SS, the entire system in FIG. 1 constitutes a system in accordance with the invention. If the routing digital address insertion circuits are also contained in these stations SS, then all the system nodes, namely concentrators CO, local exchanges LE and transit exchanges TE become switching networks in compliance with the invention and the links CL, EL and TL are input links to and output links from these switching networks. As an input link, they may have at least one channel but as an output link they must have a plurality of channels (channel group or channel bundle). However, and still within the scope of the invention, the address insertion into the addresses field can be transferred to the concentrator CO or local exchange LE level." 3:3-36.
generating means for generating a train of frames	The '311 Patent discloses a generating means for generating a train of frames.

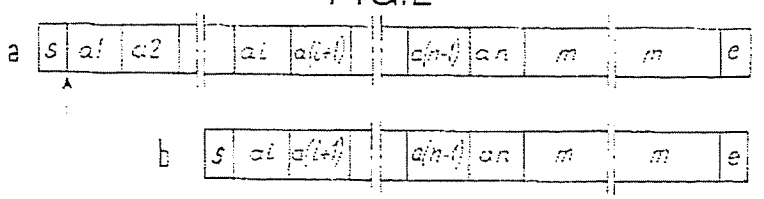
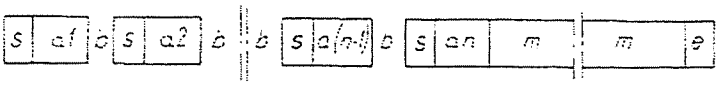
	"Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a. It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit comprises means for deleting the address concerning itself in the address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its route. The address intended for a directional switching unit

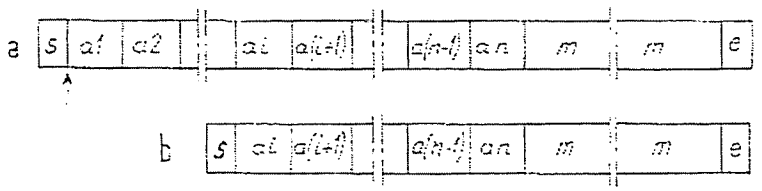
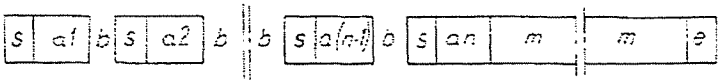
	encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
wherein each frame	The '311 Patent discloses that each frame includes a transmission

includes a transmission overhead field containing timing information and an empty payload field,	overhead field containing frame timing information and an empty payload field. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "It will be stated that a packet such as this is "self-routed" since it includes all the indications essential to its passage through the system. The word s will advise each directional switch encountered of the arrival of a packet that must switch in real time along a free channel in its output bundle or in one of its output bundles. The word e will advise it that it can free the channel that was tied up during the packet flow. It should be recalled that the address fields are intended for the respective directional switching units, the packet is to meet during its passage and not for the switching networks themselves that can encompass one or several directional switching units. The address field can only relate to the directional switching units included in the switching networks. The directional switching units may be designed as one of two versions. In the first (referred to as "address-saving" directional switching unit), the packet keeps its initial field from one end to the other of its route; it thus remains in keeping with diagram 2a. It must however also include a "pointer" positioned as indicated by an arrow, i.e. between the words s and a1. The value of this pointer is incremented by unity steps upon passing through each directional switching unit encountered to enable the next directional switching unit to recognize the output bundle concerning it from the rank thereof. In the second version, consideration is taken into account of the fact that the addresses already used during packet switching operations become useless and each directional switching unit comprises means for deleting the address concerning itself in the

	address field of the packet it receives and retransmits. The address in the address field, therefore shortens as the packet follows its route. The address intended for a directional switching unit encountered is always located in the first packet address field, thereby doing away with any need for a pointer. The address field may for instance, have the make-up given by diagram 2b in FIG. 2 upon leaving the switching unit with an address a (i-1). It now contains only those addresses with indices at least equal to i. The address ai will disappear when traveling through the following directional switching unit. The deletion of an address causes deletion of the start word s of the start field of the packet that precedes this address. This word s must be reintroduced by the directional switching unit prior to retransmission of the packet." 3:43-4:31 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4.

	FIG.2  FIG.3 
Processing means for processing data from a plurality of sources into packet format, and	The '311 Patent discloses a processing means for processing data from a plurality of sources into packet format. "The present invention concerns a telecommunication network for transmitting, receiving and switching digital data packets and, more particularly, a packet-switching network of the multiservice type. Multiservice packet networks serve to transmit, between multiservice subscribers, packets of digital data of different nature for example packetized speech data, visiophony image and sound data and digital information data. Such data originate from several digital data transmit equipments and are intended to digital data receive equipments, the said equipments being located in the subscriber's stations." 1:10-22 "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination; m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in

	memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 
Inserting means for receiving said train of frames and for inserting each of said packets comprised of data from one of said plurality of sources into any empty payload field of any of said frames available to said inserting means to form said bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit	The '311 Patent discloses an inserting means for receiving said train of frames and for inserting each of said packets comprised of data from one of said plurality of sources into any empty payload field of any of said frames available to said inserting means to form said bit stream so that data from each of said sources can be transmitted at its own desired bit rate via said bit stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream. "Diagram 2a of FIG. 2 gives an example of such a complete packet that comprises the words of groups of words as in the following chronological order: s: packet start word; a1, a2, . . . an: routing words or fields designating the outputs of the switching network through which the packet must travel to reach its destination;

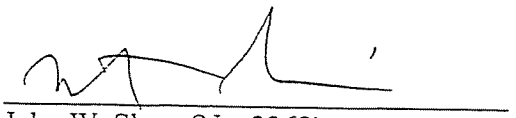
stream and so that data from said plurality of sources can be transmitted simultaneously via said bit stream.	m: message fragment constituting the packet information field; e: packet end word." 3:42-52 "When control wire 321' transmits a pulse at the same time as a connection signal appears along wire 403, then control circuit 620 triggered by logic circuit 650 causes the address carried via bus 400 to be stored in register 630, or in other words, this register 630 stores the destination of the packet that will be stored in memory 610. When a channel in the destination outgoing bundle becomes free, comparator 640 checks the identity of the address stored in register 630 and the address routed via bus 400. Logic circuit 650 checks via its input 652 which is linked to wire 403, that it is indeed a disconnection and that the disconnection order is not an order sent to the memory channel in question (input 651 connected to the output wire 321') at the end of packet storing. Circuit 650 then delivers a bus request to circuit 250 via flip-flop 660 and gate 680 whereas circuit 670 sets a connection signal via its output 673 in the direction of bus 400. Flip-flop 660 supplies the signals outgoing from logic circuit 650 when a new packet storing signal arrives and stops the signals that might appear after reception of the signal for releasing a channel in the destination bundle and after initialization of the packet transmission." 17:50-18:4. FIG.2  FIG.3 

Claim of U.S. Patent No. 4,893,306	**Disclosure in Hoberecht, "A Layered Network Protocol for Packet Voice and Data Integration," IEEE Journal on Selected Areas in Communications, Vol. SAC-1, No. 6, December 1983 ("Hoberecht")**
1. A method for simultaneously	Hoberecht discloses a method for simultaneously transmitting data from sources having different bit rates in a

	since C0 selects are not normally used to transmit data, this is the equivalent of holding 32 Kbps of excess bandwidth in reserve until it is needed. . . . Alternately, if the timing slip is negative (that is the external clock is slower than the port clock so that less data is being received by the SCC 10 from DCE 14 than is being transmitted from the SCC 10 to the satellite link), then on the following data select (select 2, scan 1 of FIG. 4), no data is read from the transmit RAM 20 and the read pointer 24 is not incremented. This effectively slows down the RAM 20 read rate so as to match the write rate. The C0 select of scan 1 will transmit a negative slip code as can be seen in Table 1.") *See, e.g.*, 5:49-52 ("In the following C0 select (scan 2 of FIG. 4), the contents of the register file word 0 are read by the digital switch in the SCC 10 and that information is transmitted via the satellite link to the SCC 12 at station 1.") *See, e.g.*, 5:56-69 ("In the following C0 select (scan 3 of FIG. 4), the word 0 location is read again by the digital switch in the transmit logic of FIG. 2, and that value is transmitted via the satellite link to the destination SCC 12 at station 1. The transmitted value relates the time of occurrence of SN with the time of occurrence of the 250 microsecond clock. What has effectively been done is to determine what the difference is between the N and the N' counter values with respect to the 250 microsecond clock boundaries following the occurrence of SN. SN was chosen as a one kHz signal so as to save space capacity. A higher frequency of SN can be used, however it will consume more bandwidth.")

Lucent reserves the right to supplement its response to this Interrogatory based on ongoing discovery and claim construction proceedings.

YOUNG CONAWAY STARGATT & TAYLOR, LLP



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Dated: May 15, 2006

EXHIBIT 7

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC. Plaintiff/Counterclaim Defendant, v. CISCO SYSTEMS, INC. Defendant/Counterclaim Plaintiff.	)	Civil Action No. 04-876-GMS

CISCO'S SUPPLEMENTAL RESPONSES TO INTERROGATORY NOS. 1, 2, 5-7, AND 9-11

Pursuant to Rule 33 of the Federal Rules of Civil Procedure, defendant Cisco Systems, Inc. ("Cisco") supplementally objects and responds to plaintiff Telcordia Technologies, Inc. ("Telcordia") Interrogatory Nos. 1-2, 5-7 and 9-11 as follows:

GENERAL OBJECTIONS AND OBJECTIONS TO INSTRUCTIONS

1. Cisco objects to each interrogatory to the extent it seeks information protected by the attorney-client privilege, the work-product doctrine, or any other applicable privilege or immunity. Nothing contained in Cisco's responses is intended to be, or in any way shall be deemed, a waiver of any such applicable privilege, doctrine, or immunity.

2. Nothing in these responses is an admission by Cisco of the existence, relevance, or admissibility of any information, for any purpose, or the truth or accuracy of any statement or characterization contained in any interrogatory. Cisco reserves all objections and other questions as to competency, relevance, materiality, privilege, or admissibility related to the use of its responses and any document or thing identified in its responses as evidence for any purpose whatsoever in any subsequent proceeding in this trial or any other action.

witnesses knowledgeable about the products and functionalities accused of infringement in this case.

INTERROGATORY NO. 2

Separately for each different product identified in response to Interrogatory No. 1, and on a month-by-month basis up until the date of trial of this action or the date of the response to this interrogatory, whichever is later, state the results of Cisco's activities relating to the product, including (a) the total quantity made, used, sold, offered for sale, imported, exported, leased, distributed, or licensed in the United States, (b) the gross and net revenues and profits from each such activity, and (c) identification of all documents relating to such activities.

SECOND SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 2

In addition to its general objections, Cisco objects to this interrogatory as overly broad and unduly burdensome, and as vague and ambiguous. Cisco further objects to this interrogatory as not being limited in time.

Subject to and without waiving its objections, pursuant to Fed. R. Civ. P. 33(d), Cisco produced sales orders from the relevant time frame that relate to the products Telcordia is accusing of infringement. These sales orders may be found at CSCO0445-0001 and CSCO0445-0002. These sales orders show the components of each sales transaction and the revenue and direct costs associated with each component. Cisco also produced financial documents from which costs and profits associated with the products Telcordia is accusing of infringement can be derived. *See* CSCO 0445-0004 and 0008.

INTERROGATORY NO. 5

For each prior art reference that Cisco contends, whether taken separately or in combination, invalidates any claim of the Relevant Patents under 35 U.S.C. §§ 102 or 103,

identify: (a) each claim in the Relevant Patents that Cisco contends is invalidated by the reference(s); (b) each fact known by Cisco that supports or refutes its contentions that each and every claim element or limitation is disclosed or suggested by specific teachings in the prior art reference; (c) all current or former officers, employees, agents, and consultants retained by or for Cisco who are most knowledgeable about each identified item of prior art and its relationship to any of the Relevant Patents; and (d) all documents relating to such prior art or Cisco's contentions.

THIRD SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 5

In addition to its general objections, Cisco objects to this interrogatory to the extent it seeks information protected by the attorney-client privilege or the work-product doctrine. Cisco further objects to this interrogatory as overly broad and unduly burdensome, and as vague and ambiguous. Cisco further objects to this interrogatory to the extent that it seeks information neither relevant to the claims or defenses in this litigation nor reasonably calculated to lead to the discovery of admissible evidence. Cisco further objects to this interrogatory as premature because the claims have not been construed as a matter of law, and fact and expert discovery have not closed.

Subject to and without waiving its objections, Cisco states that the following prior art, alone or in combination, includes all of the limitations of, and therefore invalidates, one or more of the claims of the '306, the '633, and the '763 Patents under 35 U.S.C. § 102 and/or 35 U.S.C. § 103. Cisco provides this response with the understanding that Telcordia has received disclosures from Alcatel and Lucent in *Telcordia Technologies, Inc. v. Alcatel*, Civil Action No. 04-874-GMS (D. Del.) and *Telcordia Technologies, Inc. v. Lucent Technologies, Inc.*, Civil Action No. 04-875-GMS (D. Del.), and this response does not necessarily repeat each fact,

transmitting data from said plurality of sources simultaneously via said bit stream.[8] *See, e.g., id.* at 9:6-8; 9:33-46; 7:35-40 ("Since each packet contains all of the information necessary to route a packet, and since the packets work synchronously with the DS-1 standard, both data as well as voice communication can be supported in a packetized format in essentially real time.").

In yet another example, the asserted claims of '306 Patent are anticipated by FasNet, as described in a number of publications including, *inter alia*, *Description of FasNet—A Unidirectional Local-Area Communications Network*, authored by J.O. Limb and C. Flores, and published in the Bell Systems Technical Journal in 1982 ("the Limb-Flores 1982 reference"). For purposes of this interrogatory response, Cisco will address FasNet as described in the Limb-Flores 1982 reference.

The Limb-Flores 1982 reference teaches that "Fasnet is an implicit token-passing, local-area network aimed at supporting high data rates and carrying a wide mix of traffic (data, voice, video and facsimile)." *See* Limb-Flores 1982 reference at Abstract; *see also, e.g., id.* at p. 1415 ("An integrated transmission system simplifies the implementation of services that utilize different types of traffic. Examples are voice annotated electronic mail and interactive use of voice and facsimile.").

The Limb-Flores 1982 reference also teaches the generation of a bit stream comprising a sequence of frames, each of said frames including a transmission overhead field containing frame timing information and an empty payload field.[9] *See, e.g., id.* at p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again."); 1423-24.

[8] For the same reasons, the Baran EP Patent teaches the corresponding limitations of asserted claims 3 and 4.

[9] For the same reason, the Limb-Flores 1982 reference teaches the "generating means" limitation of asserted claim 4.

Specifically, the Limb-Flores 1982 reference describes a frame structure including a transmission overhead field containing frame timing information and an empty payload field. *See, e.g., id.* at p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (i) the frame check sequence computed on the previous fields for error detection and (ii) the access control (AC) field which determines how and when each station may access the physical medium."); Table 1 (illustrating a frame structure, which includes a transmission overhead field, and a packet, which is in the payload field); Figure 3 (illustrating a frame, including the transmission overhead field and a packet, which is in the payload field); 1423-24.

The Limb-Flores 1982 reference also discloses the filling of frames with data from a plurality of sources with access to the bit stream.[10] *See, e.g., id.* at p. 1418 ("Basic access control for Fasnet is as follows. The head station, S1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again."); p. 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream."); Figure 3 (illustrating a packet in the payload field of a frame).

Furthermore, the Limb-Flores 1982 reference discloses that data in packetized format from any of the sources is written into any available empty payload of any of said frames

[10] For the same reasons, the Limb-Flores 1982 reference teaches the "inserting said packets from said sources . . ." and "inserting means" limitations of asserted claims 3 and 4.

for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from the plurality of sources simultaneously via the bit stream.[11] *See, e.g., id.* at p. 1419 ("If a station has priority, it is given permission to access the line for an integral number of slots. In this manner, the active stations can access the line for a specified duration in the order in which they are physically located on the line."); p. 1428 ("Considering the first method, any station Si in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream."); p. 1432.

As yet another example, to the extent the patent is read to cover, as Telcordia alleges, the transmission of packetized data (e.g., ATM) over a synchronous transmission (e.g., SONET), the asserted claims of the '306 Patent are anticipated and/or rendered obvious by the work performed by CCITT Study Group XVIII "SGXVIII." SGXVIII was tasked with the creation of a standardized "Integrated Services Digital Network," or ISDN. The membership of SGXVIII discussed the use of data packets in proposed public broadband ISDN networks as early as December 1985 in its Kyoto, Japan meeting. This method was alternatively called "packet mode" or "Asynchronous Time Division (ATD)" or "New Transfer Mode." See COM XVIII-R 12-E at 71-72, 95-96, 123-126.

ATD (alternatively ATDM) refers to a method originally proposed by W.W. Chu in "A Study of Asynchronous Time Divison Multiplexing for Time Sharing Computer Systems" Proc AFIPS Vol 35, pp. 669-678, 1969. It involves inserting fixed-length cells (each cell had a header and a data field) into unassigned time slots. Jean-Pierre Coudreuse and others built a fully functional ATD system called Prelude. *See, e.g.,* A. Thomas et al. "Asynchronous Time Division Techniques: An Experimental Packet Network Integrating Video Communication" Proc. International Switching Symposium, May 1984; *see also, e.g.*, J.P. Coudreuse and M.

[11] For the same reasons, the Limb-Flores 1982 reference teaches the corresponding limitations of asserted claims 3 and 4.

Servel, "Prelude: An Asynchronous Time-Division Switched Network" Vol. 2, Proc. International Conference on Communications, June 1987.

By the 1985 Kyoto meeting, SGVXIII had also proposed that the Broadband ISDN have a frame repetition rate of 8khz (125 μsec). The assumption behind New Transfer Mode was that it would operate on this synchronous 8khz network signal. One of the groups studying the issues relating to New Transfer Mode was the Broadband Task Group (BBTG) of SGXVIII.

At the July 1986 meeting of the CCITT in Geneva Switzerland, the BBTG proposed further study for both the New Transfer Mode and a new digital hierarchy for optical networks. COM XVIII-R 19(A)-E at 4. The BBTG further noted that both New Transfer Mode and Synchronous Time Division (STD) could exist with the same layer 1 characteristics, and consequently, a synchronous frame structure should be adopted. COM XVIII-R 19(B)-E at 91.

At the same July 1986 meeting, Working Party XVIII/1 noted the relationship between New Transfer Mode and ATD. Working Party XVIII/1 considered ATD similar to the access aspects of New Transfer Mode. There were important distinctions however, and the group agreed to use the name New Transfer mode until a new name could be agreed on. COM XVIII-R 19(C)-E at 37. CCITT Subworking Party 1/2 XVIII also met in Stockholm, Sweden in September of 1986 to further discuss packet mode services, including New Transfer Mode and ATD. See Stockholm Meeting Report.

The Stockholm meeting was discussed extensively at a meeting of the T1D1.1 Broadband ISDN Subworking Group in Raleigh, North Carolina. This meeting was chaired by Glen Estes of Bell Communications Research ("Bellcore"). The meeting report discusses ATDM / New Transfer Mode and its relationship to SONET. See CCITT Working Party XVIII/1 "Stockholm Meeting Report" (September 1986) at FSI058819.

In February 1987 in Brasilia, Brazil, the BBTG issued its report to SGXVIII of the CCITT. During the Brasilia meeting, the term Asynchronous Transfer Mode ("ATM") was adopted to replace the terms New Transfer Mode and ATD in this context. See XVIII-R 34(B)-E

at 27. The various reports from the Brasilia meeting including extensive discussions of ATM, SONET, and Broadband ISDN generally. *See, e.g.,* CCITT Working Parties XVIII/1 to 5, XVIII/7, and Broadband Task Group of Study Group XVIII Report entitled "Report of the Brasilia Meeting (2-13 February 1987) of Working Parties XVIII/1 to XVIII/5, XVIII/7 and BBTG of Study Group XVIII" (February 1987) (COM XVIII-R 27-E); CCITT Working Party XVIII/1 (Service Aspects) Report entitled "Report of the Brasilia Meeting (2-13 February 1987)" (February 1987) (COM XVIII-R 28(A-C)-E); CCITT Working Party XVIII/2 (Network Aspect) Report entitled "Report of the Brasilia Meeting 2-13 February 1987, Part A" (February 1987) (COM XVIII-R 29(A)-E); CCITT Broadband Task Group (BBTG) Report entitled "Report of the Brasilia Meeting (2-13 February 1987) (February 1987) (COM XVIII-R 34(A-C)-E); CCITT Working Party XVIII/1 "Stockholm Meeting Report" (September 1996).

During the Brasilia Meeting, Mr. F. Saal of Bellcore was assigned to chair Subworking Party XVIII/BB-2 on User-Network Interfaces and Channels. The aim of XVIII/BB-2 was to allow for a user-network interface that would allow for the evolution of asynchronous transfer modes that was still consistent with existing (and possibly new) transmission hierarchies. See COM XVIII-R 34(A)-E.

During the same time, Bellcore was also involved in the development of the transmission of packetized data over a synchronous transmission, which Telcordia now alleges the asserted claims of the '306 patent cover. For example, the work of Bellcore's Broadband ISDN Task Group and the Experimental Research Prototype (ERP) project relate generally to the development of packetized data (e.g., ATM), synchronous transmissions (e.g., SYNTRAN and SONET), and the transmission of packetized data over a synchronous transmission. *See, e.g.,* Broadband ISDN Task Group Technical Report, TM-TSY-009979 (August 24, 1987); Preliminary Special Report on Broadband ISDN Access, SR-TSY-000857 (December 1987); *see also, e.g.*, deposition testimony of S.H. Lee, L.T. Wu, H.J. Chao, W.D. Sincoskie, P.E. Fleischer, C.L. Lau, among others.

As another example, the asserted claims of '306 Patent are anticipated by QPSX,

as described in a number of publications including, *inter alia*, Z.L. Budrikis and A.N. Netravali, "A Packet/Circuit Switch," AT&T Bell Laboratories Technical Journal, Vol. 63, No. 8, (Oct. 1984) ("Budrikis-Netravali"); Z.L. Budrikis, J.L. Hullett, R.M. Newman, D. Economou, F.M. Fozdar, R.D. Jeffrey, "QPSX: A Queue Packet and Synchronous Circuit Exchange," New Communications Services: A Challenge to Computer Technology, ICCC (1986) ("Budrikis-Hullett"); R.M. Newman, J.L. Hullet, "Distributed Queuing; Protocol for QPSX," New Communication Services: A Challenge to Computer Technology (1986) ("Newman-Hullett"); and U.S. Patent No. 4,922,244 ("Hullett") (collectively "QPSX references").

The QPSX references teaches that "A communications switch has been developed at the University of Western Australia that provides packet and circuit switching. The total capacity of the switch is shared flexibly between the two modes of switching." *See* Budrikis-Hullett at 288; *see also, e.g.*, Budrikis-Netravali at 1499-1502; Hullett at 2:50-57, 7:18-24.

The QPSX references also teach the generation of a bit stream comprising a sequence of frames, each of said frames including a transmission overhead field containing frame timing information and an empty payload field.[12] *See, e.g.*, Budrikis-Netravali at 1501, 1506, 1513, 1519, Figure 5; Budrikis-Hullett at 289-90, Figure 4; Hullett at 5:52-6:23, 6:38-50, 6:58-7:17, 20:42-48, Figure 6, Figure 26.

Specifically, The QPSX references describe a "frame of 125 microseconds (the telephone sampling period)" which is "subdivided into fixed length packet slots," where "two bits in every packet are used for synchronization" and "a further six bits make up an access control field." *See, e.g.*, Budrikis-Netravali at 1501, 1506, 1513, 1519, Figure 5; Budrikis-Hullett at 289; Hullett at 5:52-6:23, 6:38-50, 6:58-7:17, 20:42-48, Figure 6, Figure 26.

The QPSX references also teach the filling of frames with data from a plurality of sources with access to the bit stream.[13] *See, e.g.*, Budrikis-Netravali at 1501, 1502, 1514, Figure

[12] For the same reason, the QPSX references teach the "generating means" limitation of asserted claim 4.

[13] For the same reasons, the QPSX references teach the "inserting said packets from said sources . . ." and "inserting means" limitations of asserted claims 3 and 4.

2; Budrikis-Hullett at 289-91, Figure 4, Figure 5, Figure 6; Hullett at 2:3-11, 6:24-37, 6:51-57, 7:25-37, 7:52-60, 7:64-8:15, Figure 6.

Furthermore, the QPSX references disclose that data in packetized format from any of the sources is written into any available empty payload of any of said frames for transmitting data from each of the sources at its own desired bit rate via the bit stream and for transmitting data from the plurality of sources simultaneously via the bit stream.[14] *See, e.g.*, Budrikis-Netravali at 1508, 1510, 1518, Figure 7; Budrikis-Hullett at 289-91, Figure 6; Hullett at 1:62-2:2, 2:50-57, 4:25-27, 7:25-51, 8:16-28, 9:1-14, 9:45-54, 9:63-10:3, 13:64-65, Figure 8.

In a further example, the asserted claims of '306 Patent are anticipated by the work of Mark Beckner, Steven Minzer, and others at Bellcore, as described in a number of publications including, *inter alia*, M. Beckner, "Packet-Mode Access Capability In A Broadband Interface Structure," T1.D1.185-098, Bell Communications Research (1985) ("Beckner"); M. Beckner and S. Minzer, "A Tutorial on Asynchronous Time Division Multiplexing (ATDM): A Packet Access Capability for Broadband Interfaces to ISDNs," Bell Communications Research (Nov. 11, 1985) ("Tutorial"); and Mark Beckner and Steven Minzer, "Proposal for Inclusion of a Packet-Mode Access Capability in Broadband Interfaces to ISDNs," T1.D185-113, Bell Communications Research (1985) ("Beckner-Minzer") (collectively "Beckner-Minzer references").

The Beckner-Minzer references teach a method for simultaneously transmitting data from sources having different bit rates in a telecommunication network. *See, e.g.*, Beckner at 4; Beckner-Minzer at 2; Tutorial at 2-3, Figure 4, Figure 5.

The Beckner-Minzer references also teach the generation of a bit stream comprising a sequence of frames, each of said frames including a transmission overhead field containing frame timing information and an empty payload field.[15] *See, e.g.*, Beckner at 2-4;

[14] For the same reasons, the QPSX references teach the corresponding limitations of asserted claims 3 and 4.

[15] For the same reason, the Beckner-Minzer references teach the "generating means" limitation of asserted claim 4.

Cisco expressly reserves the right to supplement its response to this interrogatory as Cisco's discovery and investigation in connection with this litigation continue.

Dated: May 26, 2006

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CERTIFICATE OF SERVICE

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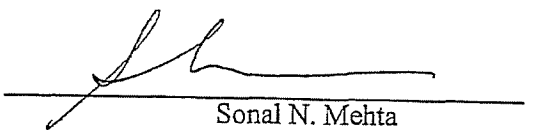

Sonal N. Mehta

EXHIBIT 8

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC., Plaintiff, v. LUCENT TECHNOLOGIES INC., Defendant.	)	Civil Action No. 04-875 GMS

TELCORDIA TECHNOLOGIES, INC.'S FIRST SUPPLEMENTAL RESPONSES TO LUCENT TECHNOLOGIES INC.'S SECOND SET OF INTERROGATORIES (NOS. 8-9)

GENERAL OBJECTIONS

1. Telcordia Technologies, Inc. ("Telcordia") objects to each interrogatory to the extent it seeks to require Telcordia to answer on behalf of any other person or entity. Telcordia responds to these interrogatories on its own behalf only.

2. Telcordia objects to each definition, instruction, and interrogatory to the extent it would require Telcordia to respond beyond that required by the Federal Rules of Civil Procedure or this Court's Local Rules.

3. Telcordia objects to Lucent's interrogatories to the extent they seek third-party information in Telcordia's possession, custody, or control that is subject to agreement, court order, or other duty preventing disclosure to Lucent. Telcordia objects to responding to propounded interrogatories that require the disclosure of trade secrets or other proprietary and confidential information of third parties unless Telcordia receives permission to disclose such information from such third parties or is otherwise compelled to produce the information by court order.

Claim 33	ITU-T I.363.1 Standard
(c) counting, at the source node, the derived network clock cycles modulo 16 in an RTS period; and	The circuit of Fig. 6 has a "P-bit counter C_t" that counts the derived network clock cycles in an RTS period. Since the RTS length is 4 bits, "P" equals 4 so the P-bit counter is a 4-bit counter which counts modulo 16. P. 15.
(d) transmitting from the source node an RTS that is equal to the modulo 16 count of derived network clock cycles in the RTS period.	"The 4-bit RTS is transmitted in the serial bit stream provided by the CSI bit in successive SAR-PDU headers." P. 16. Since the RTS is produced by the 4-bit counter C_t (Fig. 6), it represents a modulo 16 count of derived network clock cycles in the RTS period.

Pursuant to Rule 33(d) of the Federal Rules of Civil Procedure, Telcordia has produced, and will continue to produce, copies of documents in Telcordia's possession, custody, or control that are not otherwise protected by privilege exceptions and can be produced without violation of a court order or agreement, and from which information responsive to this interrogatory may be derived or ascertained, to the extent such documents exist.

INTERROGATORY NO. 9:

To the extent that Telcordia contends that any of the prior art references identified in Lucent's responses to Telcordia's Interrogatory No. 6 do not render the asserted claims of the Patents-in-suit invalid as anticipated and/or obvious, for each such prior art reference describe with full particularity the complete factual and legal bases for Telcordia's contentions, including (1) an identification of each claim element that Telcordia contends is not present and/or disclosed in each claim chart provided in Lucent's responses to Telcordia's Interrogatory No. 6, the complete factual and/or legal bases for any such contentions, and to the extent Telcordia contends that any part of any such Lucent claim chart is incorrect, an explanation of why it is incorrect and any factual and/or legal bases supporting such contentions; (2) an identification of all documents (by bates number) that support and/or refute Telcordia's contentions; and (3) the identification of all persons having knowledge relating to your contentions and a description in full detail of the nature of each such person's knowledge.

FIRST SUPPLEMENTAL RESPONSE:

Telcordia incorporates by reference each of the applicable general objections as though fully set forth herein.

Telcordia objects to this interrogatory as unduly burdensome to the extent it prematurely seeks the disclosure of information, such as claim charts and claim constructions, at this early stage of discovery and prior to a time set for disclosure of such information by a court scheduling order or by a schedule set by the mutual agreement of the parties.

Telcordia objects to this interrogatory to the extent it seeks to shift the burden of production and proof away from Lucent's burden to demonstrate invalidity by clear and convincing evidence.

Telcordia objects to this interrogatory as premature to the extent discovery of Lucent's documents, materials, and information is needed to respond.

Telcordia objects to this interrogatory to the extent it seeks information that is protected by the attorney-client privilege or by the attorney work product immunity.

Because it consists of multiple parts and sub-parts, Interrogatory No. 9 is improperly listed as a single interrogatory.

Telcordia objects to this interrogatory as it prematurely seeks expert disclosures outside of the schedule established by the Court.

Telcordia objects to the phrase "any of the prior art references identified in Lucent's responses to Telcordia's Interrogatory No. 6" as being vague and unduly burdensome for the following reasons:

(1) The references subject to Interrogatory No. 9 are unclear because Lucent has previously supplemented its response to Telcordia's Interrogatory No. 6.

(2) Telcordia understands Interrogatory No. 9 to be limited in scope literally to only those references in Lucent's answer to Telcordia Interrogatory No. 6 for which Lucent has provided claim charts. Otherwise, this interrogatory would be unduly burdensome as Lucent has identified numerous references in response to Telcordia's Interrogatory No. 6, but has only provided claim charts for a small subset of them against the '306 and '763 patents and for none of them against the '633 patent. Even for this small subset of the references, Lucent has failed to show how the cited and/or quoted text from the references disclose and/or suggest the corresponding claim elements in the claim charts. Thus, Lucent through this interrogatory improperly attempts to shift Lucent's burden of proof on patent invalidity onto Telcordia. Accordingly, Telcordia's responses will specifically address only those claims and references for which Lucent has provided claim charts, to the extent Telcordia can reasonably understand the bases for Lucent's invalidity positions as set forth in the claim charts.

Telcordia objects to this Interrogatory as being vague with regard to "obvious" where Lucent has not presented a *prima facie* case of obviousness in response to Telcordia's Interrogatory No. 6. Moreover, Telcordia does not view this interrogatory as seeking facts or contentions regarding secondary considerations of obviousness.

Subject to and without waiving any of these general and specific objections and reserving its right to supplement its response as discovery proceeds, Telcordia responds to this interrogatory as follows:

None of the references identified in Lucent's responses Telcordia's Interrogatory No. 6, alone or in combination with each other, disclose and/or suggest each and every element of the claims of the '306 patent or the '763 patent.

The '306 Patent

U.S. Patent No. 4,569,041, entitled "Integrated Circuit/Packet Switching System," issued to Takeuchi ("the Takeuchi '041 patent")

The Takeuchi '041 patent is directed to a network of nodes that are interconnected by one or more links in a ring configuration. Each node communicates with other nodes on the ring by writing information into recurring frames that travel around the ring during each frame cycle. At each node, circuit-switched and packet information is formatted in a packet form referred to by the Takeuchi '041 patent as "composite packet," where a portion of each composite packet is dedicated to circuit-switched information and another portion of the packet is dedicated to packet information. Each frame is divided into a plurality of time slots (referred to by the Takeuchi '041 patent as "time baskets"), and each node writes the information formatted in composite packet form each frame cycle into free time slots passing through the node. Nodes communicate circuit-switched information between each other using dedicated time slots.

The Takeuchi '041 patent does not disclose and/or suggest each and every element of the claims of the '306 patent. For example, the Takeuchi '041 patent does not describe or teach the "filling" step of claim 1 at least because 1) the system of the Takeuchi '041 patent does not write data in packetized format from any source, including circuit sources, into any available empty payload field, and 2) the system is incapable of transmitting data from each of said sources at its own desired bit rate via said bit stream. The Takeuchi '041 patent also does not disclose the "inserting" step of claim 3 at least because 1) the system of the Takeuchi '041 patent does not insert packets from any of said sources into any available empty payload field, and 2) the system is incapable of transmitting data from each of said sources at its own desired bit rate via said bit stream. *See, e.g.*, the Takeuchi '041 patent, column 11, lines 1-40 ("When nodes A and B intend

The frame is then packetized by the VDP 103, queued and reintroduced onto the MUXBUS 90 during an assigned packet mode frame. Each packet is read or ignored by each of the units or cards connected to the MUXBUS 90 as hereinafter explained, based on a time slot allocation of a synchronous bus cycle. The packet contains the destination address. The packet is eventually read by a transceiver which passes the packet to an internal trunk line for distribution through the network 12 (FIG. 1) to the destination designated in its packet address.").

See also, e.g., the Baran '979, column 19, lines 1-9 ("The transmitter circuit RAM 192 and the transmitter packet FIFO 194 are coupled to a transmit control unit 198 through which either transmitted TDM signals or transmitted packets are routed to a frame and signaling inserter 200. The frame and signaling inserter 200 inserts the DS-1 framing signals into the TDM signals or into the packets in accordance with conventional trunk system technology.").

Further, Lucent has failed to provide any indication as to how or why the remainder of the references Lucent cites against the '306 patent remedy the deficiencies of the Baran '979.

Limb & Flores, "Description of Fasnet-- A Unidirectional Local-Area Communications Network," The Bell System Technical Journal, Vol. 61, No. 7, September 1982 ("the Limb & Flores Fasnet reference")

The Limb & Flores Fasnet reference is directed to a token-passing, local area network referred to as Fasnet, where a plurality of stations are connected to two unidirectional lines. "One line passes all stations carrying traffic in one direction and the other line passes all stations carrying traffic in the other direction." [p. 1416] Each station communicates with other stations by writing information into free slots traveling on the lines. "The access method is closely related to a ring protocol (e.g., see Ref. 7) and may be regarded as a variant of implicit token passing." [p. 1414]

The Limb & Flores Fasnet reference does not disclose and/or suggest each and every element of the claims of the '306 patent. For example, the Limb & Flores Fasnet reference does not describe or teach the "generating" and "filling" steps of claim 1 at least because 1) the Fasnet system does not generate a bit stream that includes a sequence of frames each including a transmission overhead field containing frame timing information and an empty payload field, 2) the Fasnet system does not write data in packetized format from any source, including circuit sources, into any available empty payload field, and 3) the Fasnet system is incapable of transmitting data from each of said sources at its own desired bit rate via said bit stream.

The Limb & Flores Fasnet reference also does not disclose the "generating" and "inserting" steps of claim 3 at least because 1) the Fasnet system does not generate a bit stream that includes a sequence of frames each including a transmission overhead field containing frame timing information and an empty payload field, 2) the Fasnet system does not insert a packet from any of said sources into any available empty payload field, and 3) the Fasnet system is incapable of transmitting data from each of said sources at its own desired bit rate via said bit stream.

See, e.g., Limb & Flores Fasnet reference, p. 1418 ("The frame structure suggested in Ref. 13 and its relation to the data link sublayers is shown in Table I. The information unit is delivered by the network layer. The logical link control appends the source address, the destination address, the link control field for windowing, acknowledgments, and similar functions. We call this unit a packet, and in the work described here we will assume it is of fixed length. The media access control sublayer appends (*i*) the frame check sequence computed on the previous fields for error detection and (*ii*) the access control (AC) field which determines

how and when each station may access the physical medium. The main objective in the design of this field is to control access among all active stations in an efficient, reliable, and fair manner. The frame start and frame end delimiters are unnecessary, since the stations are kept in tight bit and frame synchronization (see Section 5.1). The duration of the frame is referred to as a slot.").

See also, e.g., Limb & Flores Fasnet reference, p. 1418 ("Basic access control for Fasnet is as follows: The head station, S_1, initiates a cycle on line A. After a cycle has been initiated, each active station on the line with packets destined in the right direction is allowed to access the line for one slot. To do this, each station monitors the line. When it senses the line idle, it seizes the line for one slot. It has to wait for a new cycle to be initiated before it attempts to access the line again.").

See also, e.g., Limb & Flores Fasnet reference, p. 1428 ("Considering the first method, any station S_i in the WAIT state that observes END = 1 may attempt to seize any empty slots on the opposite line. The number of empty slots seized depends on the time the END = 1 frame takes to propagate to the next active station, which then seizes empty slots, thus preempting active stations downstream. The intercycle gap now depends on the propagation time from the last active station to the end station and back. (The relative timing of the frame starts in the two lines will also affect the gap size). As shown in the example of Fig. 7, the intercycle gap has been reduced from nine slots to three, shown for line A only.").

Further, Lucent has failed to provide any indication as to how or why the remainder of the references Lucent cites against the '306 patent remedy the deficiencies of the Limb & Flores Fasnet reference.

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Dated: November 11, 2005
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CERTIFICATE OF SERVICE

I hereby certify that on the 11th day of November, 2005, the attached **TELCORDIA TECHNOLOGIES, INC.'S FIRST SUPPLEMENTAL RESPONSES TO LUCENT TECHNOLOGIES INC.'S SECOND SET OF INTERROGATORIES (NOS. 8-9)** was served upon the below-named counsel of record at the address and in the manner indicated:

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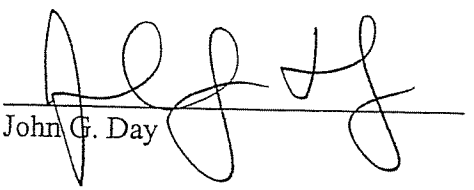

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